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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,287	09/12/2003	Feng Chen	TI-35766 (032350.B524)	7460

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EXAMINER

WILLIAMS, HOWARD L

ART UNIT PAPER NUMBER

2819

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/661,287	Applicant(s) CHEN, FENG	
	Examiner Howard L. Williams	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 5, 13 and 18-20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6-12 and 14-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

*(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.*

Claims 1-4, 6-12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Benabes et al. article (*Passive sigma-delta converter design*) in view of the Chen et al. article (*A 0.25 mW 13 b passive  $\Sigma\Delta$  modulator for a 10 MHz IF input*) and Yamakido et al. (US 5,227,795) or Voorman et al. (US 5,103,228). Benabes et al. article *Passive Sigma-Delta Converters Design* discloses a delta-sigma ADC with a continuous time passive filter (fig. 3 page 471). Benabes et al. also discloses a discrete time feedback circuit via the DAC shown in figure 1 (page 469). Benabes et al. shows in figure 2 a model of the feedback loop, input is taken as zero for figure 2, shown as a switch and hold element which is seen as reasonably suggestive of a capacitor for the hold element. Chen et al. discloses use of passive filtering delta-sigma ADC using switched capacitors in the feedback loop. Use of switched capacitor as the DAC feedback element in Benabes would have been obvious to provide a simple and compact DAC and the use of RC passive filters would provide reduced switching noise. Benabes et al. and Chen et al. don't specify whether the respective input signals are a voltage or a current signal so they don't disclose a transconductance element. Yamakido et al. and Voorman et al. disclose transconductance elements (V-I) to provide a current for summing with the feedback signal. The inclusion of a transconductance element in Benabes et al. would have been obvious because current summing is faster and more simply implemented than voltage summing.

Applicant's arguments filed 24 March 2005 have been fully considered but they are not persuasive. First, the response states the arguments previously presented are repeated. This is indeed troubling. Reviewing the previously presented arguments,

they all rely upon now disavowed first order filter and second order filter recited in the claims at that time. Since the current response now disavows this, a repetition of argument is without merit.

Below is the currently submitted argument:

The arguments previously presented are repeated. In addition, it is noted that the claims required that the continuous time circuit not only be passive, but that it contain both capacitors and resistors. Clearly, Benabes nowhere teaches or suggests the circuit as claimed either in structure format or in method format other than stating that a design for a passive sigma-delta converter is provided. The claims herein require much more. As to the Chen reference, no resistive elements are shown in any of the circuits depicted.

In addition, the claims require the combination of the passive continuous time circuit in combination with a passive discrete time stage wherein the input signal and the feedback signal are combined. There is no teaching or suggestion in any of the references not only of such a circuit, but of such a combination. While the individual circuits depicted may be in the prior art, the combination as claimed is nowhere taught or suggested.

In reality Benabe's discloses a passive continuous time delta sigma converter that has passive continuous time forward path filter depicted in figure 3. Below is figure 3 of Benabe:

This filter has real negative zeros and poles. It can be easily realized using passive filters.

One possible realization is given by the following topology

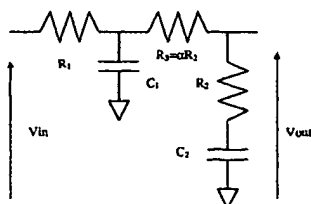


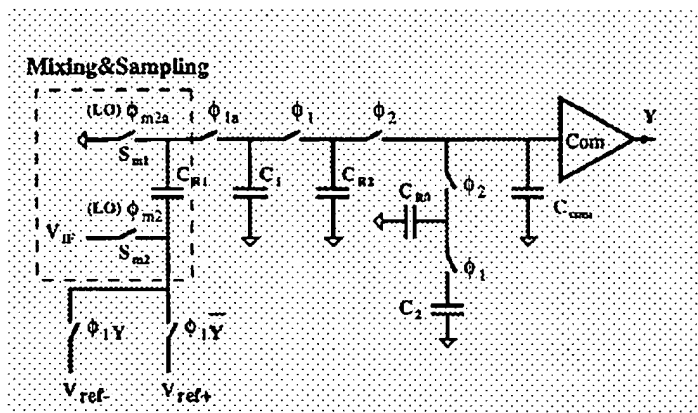
Figure 3 : Second-order modulator filter

The transfer function of Figure 3 filter can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{R_2 C_2 s + 1}{R_1 C_1 R_2 C_2 (1 + \alpha) s^2 + [R_1 C_1 + (R_1 + R_2 (1 + \alpha)) C_2] s + 1}$$

The Benabe article also includes the statement near the top of left hand column of the first page: "This approach will be applied in the case of filters using only resistors and capacitors elements." (Emphasis added). Accordingly, Benabe is seen to disclose a continuous time, passive filter using both resistors and capacitors. Benabe also provides a discrete time feedback loop noting the switch illustrated in the DAC of Fig. 1. The Chen article also uses discrete time feedback loop as seen below by the switches applying  $V_{ref-}$  and  $V_{ref+}$ . Benabe also references the Chen conference article or later journal article at the beginning of section III (Design Example) on page 470. This statement is seen as more than sufficient suggestion to combine under 35 USC 103.

The Chen article provides in figure 2:



The element  $C_{R2}$  and the two switches clocked on  $\Phi_1$  and  $\Phi_2$  simulate a resistor as well known in switched capacitor technology. Capacitor  $C_{R0}$  and its two closest switches function likewise. The choice of subscripts for these two capacitors supports this reading. If one were to redraw the Chen article figure 2 circuit replacing the capacitors  $C_{R2}$ ,  $C_{R0}$  and the adjacent switches one pretty much gets a single line figure 2 of the present application. Accordingly the rejection will be maintained.


Claims 5, 13 and 18-20 are allowable over the art of record which is not noted as disclosing the particular capacitance ratio recited in these claims.

Application/Control Number: 10/661,287  
Your Reference: TI-35766 (032350.B524)  
Art Unit: 2819

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Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 703-872-9306.

1 April 2005  
Voice 571.272.1815

  
Howard L. Williams  
Primary Examiner  
Art Unit 2819